Amendments to the Claims:

This listing of the claims will replace all prior version, and listings, of the claims in the application:

Listing of the Claims:

1. (Currently Amended) A memory controller for use in a system having a program-addressable memory controlled by the memory controller and a processor coupled with the memory by an external bus, the memory controller comprising a compression map cache to store information that identifies a compressed cache line's worth of information stored in the memory, the compressed cache line's worth of information comprising a compressed version of a first cache line's worth of information and a compressed version of a second cache line's worth of information, said memory controller including storage space to identify physical continuous addressing space of the program addressable memory in which a compression map is stored.

2. (Cancelled).

3. (Previously Presented) The memory controller of claim 1, wherein the information comprises a bit for each block of a plurality of blocks of memory space of the memory, wherein each of the plurality blocks stores its own cache line's worth of information, the bit to indicate whether its corresponding block is storing a compressed cache line's worth of information.

4. (Cancelled).

5. (Previously Presented) The memory controller of claim 3, wherein, when all bits of the corresponding block is storing a same value, the value is identified in the information.

6. (Previously Presented) The memory controller of claim 5, wherein the value is a value of 0.

7. (Previously Presented) The memory controller of claim 1, wherein the information comprises a bit for each macro block of a plurality of macro blocks of memory space of the memory, where each macro block of memory space of the memory stores a cache lines' worth of information for a set of companion cache lines' worth of information, the bit to indicate whether the companion cache lines' worth of information of its corresponding macro block have been compressed.

8. (Cancelled).

9. (Previously Presented) The memory controller of claim 7, wherein, when all bits of the compressed companion cache lines' worth of information are storing a same value, the value is identified in the information.

10. (Previously Presented) The memory controller of claim 9, wherein the value is a value of 0.

11. (Cancelled).

12. (Currently Amended) The memory controller of claim [[11]], wherein the [[memory]] storage space is to be written to by a computing system's BIOS.

13. (Previously Presented) The memory controller of claim 1 further comprising a scheduler to schedule requests made to the memory controller, the scheduler coupled to the compression map cache to refer to the information to determine whether a request's corresponding cache line's worth of information is stored in the memory in a compressed state.

14. (Previously Presented) The memory controller of claim 1 further comprising a first read path that flows through decompression logic circuitry and a second read path that bypasses the decompression logic circuitry, the decompression logic circuitry to decompress a compressed cache line's worth of information that has been read from the memory when a request's corresponding cache line's worth of information is stored in memory in a compressed state.

15. (Previously Presented) The memory controller of claim 1 further comprising compression logic circuitry coupled to a queue for queuing the requests, the compression logic circuitry to compress an uncompressed cache line's worth of information with a companion of the uncompressed cache line's worth of information.

16. (Previously Presented) The memory controller of claim 15, wherein the compression logic circuitry is further coupled to a second queue for queuing responses to the requests.

17. (Currently Amended) A processor and a memory controller integrated on a same semiconductor die, the memory controller controlling a program-addressable memory coupled with the processor by an external bus, the memory controller comprising a compression map cache to store information that identifies a compressed cache line's worth of information stored in the memory, the compressed cache line's worth of information comprising a compressed version of a first cache line's worth of information and a compressed version of a second cache line's worth of information, the memory controller including a scheduler to schedule requests made to the memory controller, the scheduler coupled to the compression map cache to refer to the information so that it can be understood whether a request's corresponding cache line's worth of information is stored in the program addressable memory in a compressed state.

18. (Previously Presented) The processor and memory controller of claim 17, wherein the information comprises a bit for each block of a plurality of blocks of memory space of the memory, each block of memory space of the memory to store its own cache line's worth of information, the bit to indicate whether its corresponding block is storing a compressed cache line's worth of information.

19. (Cancelled).

20. (Previously Presented) The processor and memory controller of claim 18, wherein, when all bits of the corresponding block is storing a same value, the value is identified in the information.

21. (Previously Presented) The processor and memory controller of claim 20, wherein the value is a value of 0.

22. (Previously Presented) The processor and memory controller of claim 17, wherein the information comprises a bit for each macro block of a plurality of macro blocks of memory space of the memory, each macro block of memory space of the memory to store cache lines' worth of information for a set of companion cache lines' worth of information, the bit to indicate whether the companion cache lines' worth of information of its corresponding macro block have been compressed.

23. (Cancelled).

24. (Previously Presented) The processor and memory controller of claim 22, wherein, when all bits of the compressed companion cache lines' worth of information are storing a same value, the value is identified in the information.

25. (Previously Presented) The processor and memory controller of claim 20, wherein the value is a value of 0.

26. (Previously Presented) The processor and memory controller of claim 17 further comprising memory space to identify physical continuous addressing space of the memory in which a compression map is stored.

27. (Previously Presented) The processor and memory controller of claim 26, wherein the memory space is to be written to by a computing system's BIOS.

28. (Cancelled).

29. (Previously Presented) The processor and memory controller of claim 17 further comprising a first read path that flows through decompression logic circuitry and a second read path that bypasses the decompression logic circuitry, the decompression logic circuitry to decompress a compressed cache line's worth of information that has been read from the memory when a request's corresponding cache line's worth of information is stored in the memory in a compressed state.

30. (Previously Presented) The processor and memory controller of claim 17 further comprising compression logic circuitry coupled to a queue for queuing the requests, the compression logic circuitry to compress an uncompressed cache line's worth of information with a companion of the uncompressed cache line's worth of information.

31. (Previously Presented) The processor and memory controller of claim 30, wherein the compression logic circuitry is further coupled to a second queue for queuing responses to the requests.

32. (Previously Presented) The processor and memory controller of claim 17, wherein the processor comprises a cache controller with compression logic circuitry, the compression logic circuitry to compress the first cache line's worth of information with the second cache line's worth of information to form the compressed cache line's worth of information.

33. (Currently Amended) A computing system comprising:

a) a program-addressable memory; and

b) a processor and a memory controller integrated on a same semiconductor die, the memory controller controlling the memory, the memory controller comprising a compression map cache to store information that identifies a compressed cache line's worth of information stored in the memory, the compressed cache line's worth of information comprising a compressed version of a first cache line's worth of information and a compressed version of a second cache line's worth of information, the memory controller including storage space to identify physical continuous addressing space of the program addressable memory in which a compression map is stored.

34. (Previously Presented) The computing system of claim 33, wherein the information comprises a bit for each block of a plurality of blocks of memory space within the memory, each block of memory space to store its own cache line's worth of information, the bit to indicate whether its corresponding block is storing a compressed cache line's worth of information.

35. (Cancelled)

36. (Previously Presented) The computing system of claim 34, wherein, when all bits of the corresponding block is storing a same value, the value is identified in the information.

37. (Previously Presented) The computing system of claim 36, wherein the value is a value of 0.

38. (Previously Presented) The computing system controller of claim 33, wherein the information comprises a bit for each macro block of a plurality of macro blocks of memory space within the memory, each macro block of memory space to store cache lines' worth of information for a set of companion cache lines' worth of information, the bit to indicate whether the companion cache lines' worth of information of its corresponding macro block have been compressed.

39. (Cancelled)

40. (Previously Presented) The computing system of claim 38, wherein, when all bits of the compressed companion cache lines' worth of information are storing a same value, the value is identified in the information.

41. (Previously Presented) The computing system of claim 36, wherein the value is a value of 0.

42. (Cancelled).

43. (Currently Amended) The computing system of claim [[42]] 33, wherein the memory space is to be written to by the computing system's BIOS.

44-68 (Cancelled)

COMMENTS

The enclosed is being filed pursuant to a Request for Continued Examination (RCE) as provided under 37 CFR 1.114 and corresponding Request for Withdrawal From Issuance as provided under 37 CFR 1.313. The allowed claims as they stood at the time the issue fee was paid included claims 1 and 3-43. The Applicants have herewith: 1) canceled claims: 4, 8, 11, 19, 23, 28, 35, 39, 42; and, 2) amended claims 1, 12, 17, 33 and 43. As such claims 1, 3, 5-7, 9, 10, 12-18, 20-22, 24-27, 29-34, 36-38, 40, 41 and 43 are now pending.

In order to obviate any allegation of non-obvious type double patenting between the present application and issued patent 7,257,693 the Applicant has herewith: 1) amended each of the independent claims of the present application to include additional subject matter that appears to be distinct in view of the claimed subject matter of the '693 patent; and, 2) canceled claims directed to a type of compression.

The Applicant respectfully requests reconsideration of the present application and the allowance of all claims now presented.

If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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Robert B. O'Rourke
Reg. No. 46,972

1279 Oakmead Parkway
Sunnyvale, CA 94085-4040
(408) 720-8300